# Radiation-Hardened I/O Expansion Chip, Phase I

Completed Technology Project (2018 - 2019)

## Project Introduction

VORAGO Technologies will create a rad-hard I/O Expansion Chip for next generation spaceflight processor devices, including the High-Performance Spaceflight Computing (HPSC) Chiplet.

The I/O Expansion chip will have multiple high-speed interfaces so that it can interface with a space processor and support high speed communications. It will also have programmable-voltage-level GPIO to support both non-differential communications protocols and general I/O expansion.

The I/O expansion chip will provide dedicated hardware on the IC to support each of the communications protocols. The I/O expansion chip will also include an appropriate amount of memory and a multi-channel Direct Memory Access controller system to support simultaneous high-speed communications. To optimize power consumption, multiple PLL sources will be available on-chip to provide the appropriate clock generation for the on-chip communications controllers.

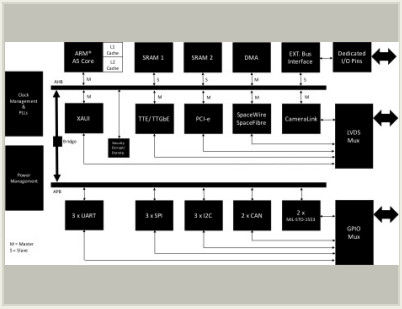
An ARM® A5 processor core will be included on the I/O Expansion Chip so that it can be used autonomously from the spaceflight processor device. This feature is expected to give the system designer good options for system level power saving modes as well as more system fault management capabilities.

The I/O Expansion chip will be implemented using VORAGO Technologies proven radiation-hardening HARDSIL® technology. HARDSIL technology will make the I/O Expansion chip immune from latch-up.

## Anticipated Benefits

This device will be an ideal companion part for next generation spaceflight processor devices, including the High-Performance Spaceflight Computing (HPSC) Chiplet. Programming the device and supporting software will be straightforward as it is based on an existing widely used ARM Cortex architecture.  Possible applications of the device would be: - I/O Expander for processors or FPGAs, - Multi-communications interface / hub for processors or FPGAs, - Network bridge for processors or FPGAs, - Standalone A5 class processor with multiple communications interfaces, - Redundant processor system for implementing additional system-level lower power modes, - Redundant processor system for implementing failsafe strategy

Based on our experience marketing ARM Cortex-M based microcontrollers to

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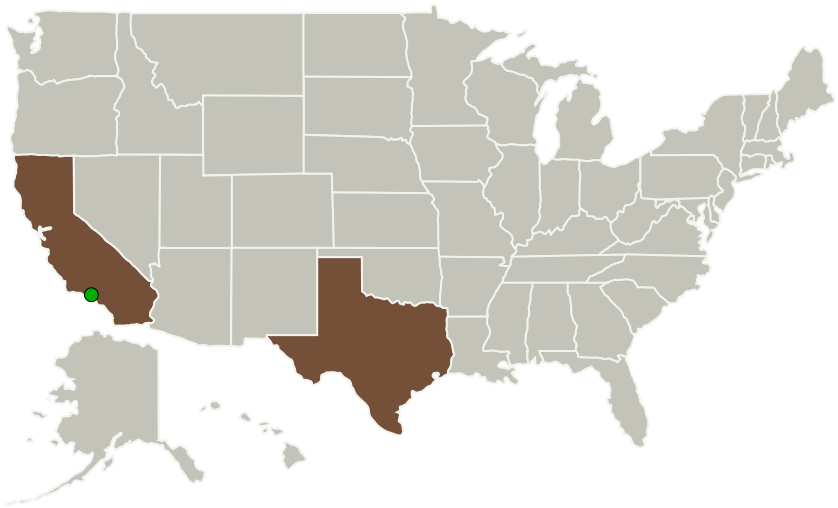
the space market, we have determined that is a demand for a device like the I/O Expander Chip for the types of applications that are stated in section 10.1. This device, implemented in CMOS and radiation-hardened by HARDSIL would be an ideal companion chip to next generation spaceflight processors as well as a cost-effective alternative to solutions such as some expensive FPGAs and SPARC-based products.

### Primary U.S. Work Locations and Key Partners



| Organizations Performing Work | Role | Type | Location |
|---|---|---|---|
| Silicon Space Technology Corporation | Lead Organization | Industry | Austin, Texas |
| Jet Propulsion Laboratory(JPL) | Supporting Organization | NASA Center | Pasadena, California |

| Primary U.S. Work Locations | |
|---|---|
| California | Texas |

## Organizational Responsibility

**Responsible Mission Directorate:**

Space Technology Mission Directorate (STMD)

**Lead Organization:**

Silicon Space Technology Corporation

**Responsible Program:**

Small Business Innovation Research/Small Business Tech Transfer

## Project Management

**Program Director:**

Jason L Kessler

**Program Manager:**

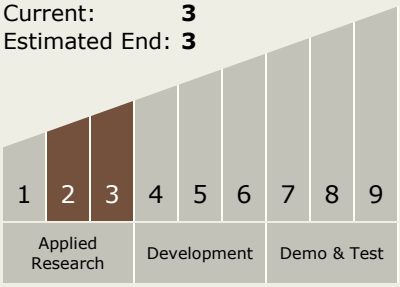
Carlos Torrez

**Principal Investigator:**

Ross Bannatyne

## Technology Maturity (TRL)

Start: **2**
Current: **3**
Estimated End: **3**



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## Project Transitions

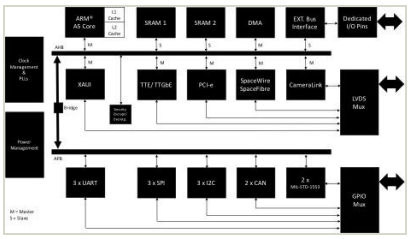
**July 2018:** Project Start

**February 2019:** Closed out

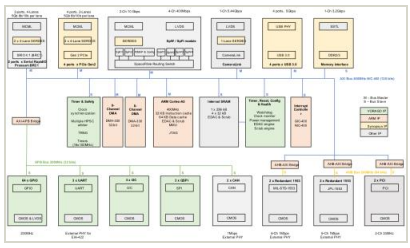
**Closeout Documentation:**

- Final Summary Chart*(https://techport.nasa.gov/file/141257)*

## Images




**Briefing Chart Image**
Radiation-Hardened I/O Expansion Chip, Phase I
*(https://techport.nasa.gov/image/129055)*



**Final Summary Chart Image**
Radiation-Hardened I/O Expansion Chip, Phase I
*(https://techport.nasa.gov/image/126185)*

## Technology Areas

**Primary:**

- TX05 Communications, Navigation, and Orbital Debris Tracking and Characterization Systems
  - TX05.5 Revolutionary Communications Technologies
    - TX05.5.2 Quantum Communications

## Target Destinations

Earth, The Moon, Mars